MRFE9S9160 LDMOS Transistor 23cm band 1.3GHz Solid State Power Amplifier (SSPA) Project

MRFE9S9160 (E is an enhanced version of MRF6S9160, but there is no difference for the RF matching and general performance) is commonly found in many old GSM base-station systems and used as a final stage power amplifier (PA) device. We have seen there are already many excellent 23cm band 1.3GHz PAs built with this transistor. The one designed by DF9IC is very popular.

MRFE9S9160 is easy to get from the Asian market, usually sold as a second-hand component, where they are removed from used base stations. That means this LDMOS transistor is super cheap compared to many other similar devices. However, there are some issues, for example, this device comes without many documents, S-parameter information and simulation models. Therefore, this makes computer-aided design is more difficult on this device.

BG0AUB, ZHAO Feng, and I seat together, well virtually as I was in the UK, and considered were we able to make an even budget 23cm band PA for an EME project. Yes, we did. After a few design iterations, we have made the FR4 substrate 23cm band MRFE9S9160 PA, and decided to open-source it. The board can be fabricated by JLC 0.8mm technology.

We have learnt a lot from this project, including high power RF related knowledge and the use of design/simulation tools. In addition, Feng had spent massive time on this – practical installation and testing work.

DF9IC has made a FR4 substrate experiment, but the result was not grate. We started from there, and further analysis his work. Feng and I considered there are rooms to improve, and FR4 should be still a solution for 23cm band PA designs. After playing with computer simulations, I decided to change the layout, so making rooms for better matching.

The following picture shows the new layout:

And a PA 3D look (Specially thanks to BG7GBC for the generation of 3D picture):

The installation process should be straightforward, and tuning process is not complex. In older to test this PA, a 28V 20A PSU is needed. Overcurrent protection one is more expected. After the solder process, the PA should be looking like as follows:

Note that the PA will produce massive heats, so a good heatsink should be given. LDMOS static current is sensitive to temperature. The bias circuit can be upgrade to temperature compensation ones as well. Our dual LDMOS power combine PA has replaced the simple biased circuit with an enhanced one.

Turning procedure:

VERY IMPORTANT, BEFORE STARTED, MAKE SURE your ground wires and PA board ground are connected properly and firmly.

Setting the bias pot, voltage, we should set the LDMOS at 1.3A quiescent current.

The positions of six 3.3pF ATC capacitors should be mounted to the PCB silk screen indicated locations.

For the input side, the 3pF variable capacitor turning is needed. A better input matching can be then obtained – input VSWR (S11) should be < 1.5.

Generally saying, when the input is around 2 Watts, the PA will consume around 8A current and output > 60 Watts. In this case, some fine tuning can be performed – moving upper/lower three ATC capacitors together left or right 1mm each time in order to obtain the maximum output.

Large signal gain of this PA is around 16-17 dB. If the PA current is under 7A where input is 2W, or even less, you will need to move these 3.3 pF lift/right harshly, 2mm or more, and try to find a point that you have a good current reading. Some bad ATC capacitor will cause the low current/power issue too, so you should consider to replace these capacitors in the case no proper power generated. A large current is a good sight of outputting expected power.

When the input power around 6W, you should see the output is nearly saturated – output compressed.

Excessive solder is not recommended for any pads, including LDMOS gate and drain pads.